Abstract of the Disclosure

The present invention is to provide an improved efficiency of transmission and reception for data in an ATM SAR (Asynchronous Transfer Mode Segmentation and Reassembly) module for a xDSL communication service chip.

The ATM SAR module comprises a memory controller controlling signals, a generation module for transmitting a CRC32 that is a block to generate 32 bits CRC (cyclic redundancy check) block necessary for an AAL-5 PDU to check a transmission error of the AAL (ATM Adaptation Layer)-5 PDU (Protocol Data unit) in a virtual channel unit, a generation module for receiving a CRC32 to check a reception error of the AAL-5 PDU, a generation modules for transmitting and receiving a CRC10 to process the OAM (Operation, Administration and Maintenance) cell, a header manager module to add and analyze an ATM header according to the virtual channel setup information of the AAL-5 PDU, an UTOPIA interface module to provide a standard connection with an external physical module, an ATM SAR state machine controlling whole operations of the ATM SAR and a packet memory to store data that the ATM SAR has to transmit or is received through the ATM SAR. Using the packet memory, data exchange between the ATM SAR and peripheral devices is optimally performed.